What is Claimed is:

1. Shared memory data transfer apparatus where a plurality of masters access one shared memory to perform data transfers, said shared memory data transfer apparatus comprising:

a plurality of master interfaces respectively connected to the master interfaces,

write butters connected to the master interfaces for retaining data written from said masters to said shared memory,

read butters connected to the master interfaces for retaining data read from said shared memory to said masters,

a FIFO provided between said master interfaces and said shared memory for storing commands from the masters directed to said shared memory in a first-in, first-out fashion, and

a shared memory interface for controlling data transfers from said write buffers to said shared memory or data transfers from said shared memory to said read buffers in accordance with commands fetched from said FIFO.

2. Shared memory access apparatus according to claim 1, comprising an arbiter for storing a plurality of simultaneously issued commands into said FIFO in a predetermined order.

3. Shared memory access apparatus according to claim 1 or 2, comprising an arbiter for referencing the command contents and rearranging the order of commands to be stored into said

FIFO.

4. Shared memory data transfer apparatus according to any one of claims 1 through 3, which issues commands to be stored into said FIFO per access to said shared memory.

5. Shared memory data transfer apparatus according to any one of claims 1 through 4, which uses a fixed burst length in an access to said shared memory.